

Preliminary Design and Implementation of the Baseline Digital Baseband Architecture for Advanced Deep Space Transponders

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This article investigates and identifies the baseline design and implementation of the digital baseband architecture for advanced deep space transponders. Trade studies on the selection of the number of bits for the analog-to-digital converter (ADC) and optimum sampling schemes are presented. In addition, the proposed optimum sampling scheme is analyzed in detail. Descriptions of possible implementations for the digital baseband (or digital front end) and digital phase-locked loop (DPLL) for carrier tracking are also described.

I. Introduction

Future NASA missions will require cheaper, smaller, and more energy-efficient spacecraft telecommunication equipment. These requirements motivated this study on advanced transponders for deep space applications. Recently, a study [1] has investigated various digital baseband architectures for future deep space transponders. Three different architectures were proposed for near-term, intermediate, and long-term solutions. The purpose of this article is to investigate and identify the baseline design and the conceptual implementation of the digital baseband architecture for a short-term solution.

The baseline architecture will use advanced digital technologies and signal-processing techniques for improved performance along with attractive functionality and adapt-

ability to mission requirements. The identified architecture should also meet the interface constraint to minimize the cost of the design. The baseline architecture was developed based on the current configuration of the Cassini Deep Space Transponder (DST) [2]. The proposed architecture will maintain the analog IF section and the automatic gain control (AGC) loop at the first IF mixer identical to the current Cassini DST. However, the second IF will be redesigned to ease the digitization of baseband functions. In addition, the command detector unit (CDU) function, along with its modifications, will be included as a whole in the advanced DST. A description of the CDU and its modifications can be found in [1].

The simplified block diagram of the baseline architecture for the receiver of the DST is shown in Fig. 1. For this baseline architecture, the analog phase-locked loop

(APLL) for carrier tracking is replaced by a hybrid digital phase-locked loop (DPLL) and the ranging signal is extracted by filtering and turning the signal around without further signal processing (analog turnaround ranging). To simplify the hardware, the sampling frequency will be selected so that it is compatible with the sampling rate requirement of the CDU. A detailed description of the baseline architecture shown in Fig. 1 can also be found in [1].

This article begins with the trade studies for the selection of the number of bits for the ADC and the optimum sampling technique. Based on the selected optimum sampling scheme, the implementation of the baseband digital front end for simplified hardware was analyzed and proposed. Next, preliminary results related to the design and conceptual implementation of the DPLL for carrier tracking are presented and discussed. Finally, the article concludes with a summary of the salient features associated with this baseline design and direction of future work.

II. Selection of Number of Bits for the ADC

The number of bits required for the ADC at the second IF will determine the setting of the power for the AGC, the carrier signal-to-noise (SNR) degradation due to quantization, and the saturation noise. This section summarizes the results presented by Nguyen.¹ The carrier SNR degradation due to digitization, Δ , in the presence of Gaussian noise, is given by Nguyen² as

$$\Delta = \left(1 + \frac{P_N}{\sigma^2} \left(1 + \frac{P_S}{P_n}\right)\right)^{-1} \quad (1)$$

where

$$\begin{aligned} \frac{P_N}{\sigma^2} &= 2 \left(K^2 + 1\right) F(K) - \frac{2K}{\sqrt{2\pi}} e^{-\frac{K^2}{2}} \\ &+ \frac{K^2}{12(M-1)^2} \left(1 - 2F(K)\right) \end{aligned} \quad (2)$$

$$\frac{P_S}{P_n} = \left(\frac{P_S}{N_0}\right) \left(\frac{2}{F_S}\right) \quad (3)$$

¹ T. M. Nguyen, "Selection of the A/D Sampling Frequency and Number of Bits for the Advanced Transponder," JPL Interoffice Memorandum 3313-92-024 (internal document), Jet Propulsion Laboratory, Pasadena, California, April 20, 1992, revised May 18, 1992.

² Ibid.

$$K = \frac{1}{LF} \quad (4)$$

$$F(K) = \frac{1}{\sqrt{2\pi}} \int_K^\infty e^{-\frac{u^2}{2}} du \quad (5)$$

Note that (P_N/σ^2) denotes the quantization noise plus saturation noise-to-carrier signal power ratio; (P_S/P_n) denotes input carrier power-to-noise power ratio; N_0 is the one-sided input noise power density; F_S is the sampling frequency; $M = 2^{N-1}$, where N is the number of bits (including sign); and LF is the loading factor defined as follows:

$$LF = \frac{\text{rms amplitude of the total input signal}}{\text{ADC saturation voltage}} \quad (6)$$

The optimum values for K for various values of N have been calculated in [3], and the corresponding optimum LF as a function of N is depicted in Fig. 2. From the optimum values of N and LF found in Fig. 2, one can calculate the corresponding values of (P_N/σ^2) using Eq. (2). Using the calculated (P_N/σ^2) together with Eq. (1), one can calculate the carrier SNR degradation due to digitization. The results are plotted in Fig. 3 for $0 \text{ dB-Hz} < P_S/N_0 < 50 \text{ dB-Hz}$ and $1 \text{ MHz} < F_S < 36 \text{ MHz}$. Note that for $0 \text{ dB-Hz} < P_S/N_0 < 50 \text{ dB-Hz}$ and $1 \text{ MHz} < F_S < 36 \text{ MHz}$, one has: $1 + P_S/P_n \approx 1$. Using this approximation, the results are shown in Fig. 3.

Therefore, to achieve the digitization with a degradation in carrier SNR of less than 0.1 dB and to meet the required dynamic range of $6N$ dB for the input carrier signal, the required number of bits is $N \geq 4$ bits. In addition, the higher the number of bits that one selects, the less susceptible to interference the signal will be.³ Consequently, the required number of bits for the ADC should be selected such that $4 \text{ bits} \leq N \leq 8 \text{ bits}$.

III. Optimum Sampling Scheme

A. Review of Current Sampling Techniques

Currently, there are several techniques for sampling the band-pass signals [4]: in-phase and quadrature (I&Q) baseband sampling with analog quadrature, I&Q sampling with analog Hilbert transform, band-pass sampling with

³ J. Berner, "Number of Bits Required in Block-V ADC," JPL Interoffice Memorandum 3338-90-048 (internal document), Jet Propulsion Laboratory, Pasadena, California, March 26, 1990.

digital quadrature mixers, and band-pass sampling with digital Hilbert transform. Based upon the investigation in [4], the band-pass sampling technique with digital quadrature mixers is recommended (see Fig. 5) for the baseline design of the advanced transponder because of the following reasons:

- (1) There are no phase and amplitude imbalances because the mixing is done in digital domain.
- (2) The digital low-pass filter (LPF) using a finite-impulse response (FIR) filter provides constant group delay that is very important for ranging and Doppler information.
- (3) Only one ADC is required.
- (4) If the sampling period is exactly $1/4F_{IF}$, then the reference of I&Q components reduces to an alternating sequence.

It will be shown later that the hardware implementation can be simplified by using the last property with some modification. Before describing how to implement the “digital front end” for the advanced transponder, the digital front end needs to be defined.

The digital front end of the transponder (see Figs. 1 and 4) is designed to accept an IF analog signal and output digital baseband I&Q components for further processing by the remainder of transponder. The purpose of the digital front end is to provide the transponder with a demodulation capability from an IF-to-baseband digital signal.

B. Conceptual Implementation of the Digital Front End

To implement the digital front end (see Fig. 4), one must set up the criteria for selecting both the optimum sampling frequency and the analog IF. First, there are several criteria for selecting the optimum sampling frequency, namely,

- (1) The hardware implementation should be simple.
- (2) The sampling frequency should be sufficiently high to meet the required number of samples per symbol for the CDU and the carrier tracking loop.
- (3) The sampling frequency should be sufficiently high to prevent aliasing of the baseband signal with the images that occur at the sampling rate.
- (4) The sampling frequency selected should meet the current specification of the analog-to-digital (A/D) technology with reasonable cost.

Based on these criteria, the sampling frequency, F_S , must be selected to satisfy the following conditions [5–7]:

$$F_S \geq 2BW \quad (7)$$

$$\frac{2}{(l+1)} \left(F_{IF} - \frac{BW}{2} \right) \leq F_S \leq \frac{2}{(l+1)} \left(F_{IF} + \frac{BW}{2} \right) \quad (8)$$

where BW is the bandwidth of the band-pass signal in hertz, F_{IF} is the center of the IF band, and l is a positive integer. In order to simplify the hardware implementation, one chooses equality in Eq. (7) and an odd integer for l in Eq. (8):

$$F_S = 2pBW \quad (9)$$

$$nF_S = F_{IF} - \frac{BW}{2} \quad (10)$$

where $p \geq 1$ and $n = (l+1)/2$.

Solving for the sampling frequency in terms of F_{IF} , one gets

$$F_S = \frac{4pF_{IF}}{(1+4np)} \quad (11)$$

for $p = 1$, Eq. (11) reduces to

$$F_S = \frac{4F_{IF}}{(1+4n)} \quad (12)$$

where n satisfies the following inequality

$$n \leq \left\lceil \frac{F_{IF}}{2BW} - \frac{1}{4} \right\rceil \quad (13)$$

where $\lceil x \rceil$ is the smallest integer that is less than or equal to x . It should be mentioned that the sampling scheme proposed is known as the under-sampling scheme. Note that, in practice, to simplify the I&Q sampling technique using digital quadrature mixers (see Fig. 5) to the configuration shown in Fig. 7(a), the sampling frequency must

be chosen as $4F_{IF}$ [8–10].⁴ However, using Eq. (12) one can avoid selecting a high sampling frequency (and hence achieve a more energy efficient spacecraft). As an example for the proposed under-sampling scheme, let the IF be 5 MHz and the bandwidth of the signal be 36 kHz; then using Eq. (13), one obtains $n \leq 69$. If one selects $n = 6$, then the sampling frequency required for this case is, from Eq. (12), $F_S = 0.8$ MHz. Figures 7(b) and (c) illustrate and compare the two sampling schemes discussed above.

Secondly, one must select the IF so that the analog circuitry in the transponder can be designed and built easily. There are several criteria for selecting the IF, namely,

- (1) The quadrature sampling error caused by spectral bands overlapping [7] must be avoided by selecting the upper cutoff frequency of the band-pass filter (BPF) equal to an integer multiple of the bandwidth, i.e.,

$$F_{IF} + \frac{BW}{2} = cBW \quad (14)$$

where c is a positive integer.

- (2) For minimum hardware implementation, F_{IF} and F_S should satisfy Eq. (12).
- (3) F_{IF} must be chosen such that the associated band-pass filter in the analog-mixing and filtering circuitry is realizable. The passband of this filter must pass the required number of sidelobes of the command signal and possibly the highest ranging clock frequency.
- (4) F_{IF} must be chosen by taking into consideration the throughput limitation of the digital filters of the digital front end.
- (5) F_{IF} must be chosen to provide minimum carrier delay variation.

To show that Eq. (12) can be used to select the sampling frequency for hardware simplification, look at the mathematical model for the uplink signal, $S(t)$:

$$S(t) = \sqrt{2P} \sin((\omega + \omega_d)t + \Theta(t) + \varphi) \quad (15)$$

where

- P = total received power
- ω = angular carrier frequency
- ω_d = Doppler angular frequency offset
- $\Theta(t)$ = phase modulation = $md(t) \sin(\omega_{SC}t) + m_R R(t)$
- φ = phase offset
- m = command modulation index
- $d(t)$ = command non-return-to-zero (NRZ) data
- ω_{SC} = command subcarrier frequency
- m_R = ranging modulation index
- $R(t)$ = ranging signal

Without loss of generality, one can set $\omega = \omega_{IF} = 2\pi F_{IF}$, $\omega_d = 0$, $\varphi = 0$, and can expand Eq. (15) to get

$$S(t) = \sqrt{2P} [\cos(\Theta(t)) \sin(2\pi F_{IF}t) + \sin(\Theta(t)) \cos(2\pi F_{IF}t)] \quad (16)$$

The first term in Eq. (16) represents the carrier component, and the second is the command signal component.

Assume that the I&Q components of Eq. (15) are extracted by using analog quadrature mixers as shown in Fig. 6. If the cutoff frequency of the LPF is such that it rejects higher-order harmonics components and passes only the first harmonic component without distortion, then the output I&Q components are

$$I(t) = \frac{1}{2} \sin(\Theta(t)) \quad (17)$$

$$Q(t) = \frac{1}{2} \cos(\Theta(t)) \quad (18)$$

Note that Eqs. (17) and (18) have been normalized by $\sqrt{2P}$. If one assumes that the ranging signal is off, then the $I(t)$ and $Q(t)$ shown in Eqs. (17) and (18) become

$$I(t) = \frac{1}{2} d(t) \sin(m \sin(\omega_{SC}t)) \approx d(t) J_1(m) \sin(\omega_{SC}t) \quad (19)$$

$$Q(t) = \frac{1}{2} \cos(m \sin(\omega_{SC}t)) \approx \frac{1}{2} J_0(m) \quad (20)$$

⁴M. J. Agan and C. R. Pasqualino, "AMT Modem Digital Front End," JPL Interoffice Memorandum AMT:331-5-90-0 (internal document), Jet Propulsion Laboratory, Pasadena, California, October 1990.

Note that the I -component contains the command information and the Q -component contains the amplitude of the carrier component.

A sample of the signal expressed in Eq. (16) is obtained by using the sampling frequency derived in Eq. (12). At this sampling frequency, one has

$$t = kT_S = \frac{k(4n+1)}{4F_{IF}}, \quad k = 0, 1, 2, 3, 4, \dots \quad (21)$$

where T_S denotes the sampling period. Substituting Eq. (21) into Eq. (16) and evaluating it for $k = 0, 1, 2, 3, 4, \dots$, one sees that Eq. (16) generates the following sequence:

$$\begin{aligned} & \sqrt{2P} \sin(\Theta(0)), \sqrt{2P} \cos(\Theta(T_S)), -\sqrt{2P} \sin(\Theta(2T_S)), \\ & -\sqrt{2P} \cos(\Theta(3T_S)), \sqrt{2P} \sin(\Theta(4T_S)), \\ & \sqrt{2P} \cos(\Theta(5T_S)), -\sqrt{2P} \sin(\Theta(6T_S)), \\ & -\sqrt{2P} \cos(\Theta(7T_S)), \sqrt{2P} \sin(\Theta(8T_S)), \\ & \sqrt{2P} \cos(\Theta(9T_S)), \dots \end{aligned}$$

Taking the above sequence and multiplying by the $\{1, 1, -1, -1, 1, 1, -1, -1, 1, 1, \dots\}$ sequence, one gets

$$\begin{aligned} & \sqrt{2P} \sin(\Theta(0)), \sqrt{2P} \cos(\Theta(T_S)), \sqrt{2P} \sin(\Theta(2T_S)), \\ & \sqrt{2P} \cos(\Theta(3T_S)), \sqrt{2P} \sin(\Theta(4T_S)), \\ & \sqrt{2P} \cos(\Theta(5T_S)), \sqrt{2P} \sin(\Theta(6T_S)), \\ & \sqrt{2P} \cos(\Theta(7T_S)), \sqrt{2P} \sin(\Theta(8T_S)), \\ & \sqrt{2P} \cos(\Theta(9T_S)), \dots \end{aligned}$$

Note that this sequence alternates between samples of $I(t)$ and $Q(t)$ shown in Eqs. (18) and (19) with only a scaling factor difference. The above sequence can be simply expressed as

$$\begin{aligned} & I(0), Q(T_S), I(2T_S), Q(3T_S), I(4T_S), Q(5T_S), \\ & I(6T_S), Q(7T_S), I(8T_S), Q(9T_S), \dots \end{aligned}$$

Based on these results, the optimum implementation of the digital front end for the baseline design of the advanced transponder is shown in Fig. 7. As shown in this section, using the sampling frequency derived in Eq. (12), one can simplify the hardware. The hardware simplification is exactly the same as for the case when the sampling frequency is $4F_{IF}$ [9]⁵ except when using a lower F_S , and hence lower power consumption.

IV. Design and Implementation of the Carrier Tracking Loop

A. Description of the Carrier APLL and Transformation Techniques

The block diagram of the analog carrier tracking loop for the Cassini DST is depicted in Fig. 8. Based on the current design, an architecture of the DPLL for computer simulation is developed. Presently, the analog carrier tracking loop is Type I, second order PLL with the following characteristics:

$$AK = \text{loop gain} = 2.4 \times 10^7 \quad (22)$$

$$B(S) = \frac{1}{(1 + \tau_{RC}S)}, \tau_{RC} = 1.6 \times 10^{-5} \quad (23)$$

$$F(S) = \frac{1 + \tau_2 S}{1 + \tau_1 S}, \tau_1 = 4707, \tau_2 = 0.0442 \quad (24)$$

$$V(S) = \frac{1}{(1 + \tau_V S)}, \tau_V = 1.0 \times 10^{-6} \quad (25)$$

$$K(S) = \frac{1}{S} \quad (26)$$

Note that $B(S)$ is the typical LPF, $F(S)$ is the loop filter, $V(S)$ is the rolloff filter of the voltage control oscillator (VCO), and $K(S)$ is the VCO integrator.

Let $G(S)$ be the transfer function of the analog loop defined as follows:

⁵ Ibid.

$$G(S) = B(S)F(S)V(S) \quad (27)$$

From the analog characteristics of the loop, there are four different techniques (cases 1–4) to design the equivalent digital loop

- (1) **Bilinear Transformation Method.** This method preserves the phase characteristics in the narrow pass-band when mapping the APLL into the digital domain with high sampling frequency. The mapping from analog (S -domain) to digital domain (Z -domain) can be achieved by direct substitution of the following equation into the analog transfer function [11–13]:

$$S = \frac{2}{T_s} \frac{(Z - 1)}{(Z + 1)} \quad (28)$$

- (2) **Impulse-Invariant Transformation Method.** This mapping technique preserves the impulse response at the sampling points. The relationship between the S -variable and Z -variable is given by [12,13]

$$S = \frac{(Z - 1)}{T_s Z} \quad (29)$$

However, the corresponding digital transfer function cannot be obtained by substituting Eq. (28) directly into the analog transfer function as in case (1) above. Let $g(t)$ be the impulse response of $G(S)$, i.e., $g(t) = L^{-1}\{G(S)\}$, where $L^{-1}\{\cdot\}$ denotes the inverse Laplace transform of $\{\cdot\}$. Thus, the digital approximation of the analog transfer function $G(S)$ is given by

$$G_D(Z) = T_s \left(z \{ g(t) |_{t=nT_s} \} \right) \quad (30)$$

where $z\{\cdot\}$ is the z -transform of $\{\cdot\}$. Note that the analog transfer function $G(S)$ considered in this article is defined in Eq. (27).

- (3) **Step-Invariant Transformation Method.** This method preserves the step response at the sampling

points when mapping S -domain to Z -domain. The relationship between S - and Z -variables is given in [12]:

$$S = \frac{(Z - 1)}{T_s} \quad (31)$$

Similar to case (2), the equivalent digital transfer function of the open loop cannot be found by substituting Eq. (31) directly into the analog transfer function. The relationship between the analog and digital transfer function is [12,13]

$$G_D(Z) = \frac{Z - 1}{Z} \left(z \left\{ \left[L^{-1} \left[\frac{G(S)}{S} \right] \right]_{t=nT_s} \right\} \right) \quad (32)$$

where $z\{\cdot\}$ and $G(S)$ are defined the same as above.

- (4) **Rational Transformation Method.** This mapping technique is identical to the impulse-invariant transformation technique [11,12].

B. Recursive Implementation of the Carrier DPLL

To obtain the digital approximation of the carrier APLL described in Section IV.A, each functional block in the analog loop, i.e., $B(S)$, $F(S)$, $V(S)$, and $K(S)$, can be mapped directly into the Z -domain using bilinear transformation or the composite function $B(S)F(S)V(S)$ using impulse-invariant (or step-invariant) transformation. These mappings are accomplished by applying Eqs. (28), (30), and (32), depending on the type of transformation used. Following are the recursive implementations of the digital transfer functions.

1. Recursive Implementation of $B(S)$, $F(S)$, $V(S)$, and $K(S)$ Using Bilinear Transformation. To obtain the digital approximation of the analog loop using bilinear transformation, one substitutes Eq. (28) into Eqs. (23)–(26) to get the Z -domain representations for the LPF $B(S)$, loop filter $F(S)$, VCO rolloff filter $V(S)$, and the integrator $K(S)$. The results are

$$B(Z) = \frac{(1 + Z^{-1})}{(A_{00}Z^{-1} + A_{11})} \quad (33)$$

$$F(Z) = \frac{(A_0 Z - B_0)}{(A_1 Z - B_1)} \quad (34)$$

$$K(Z) = \frac{T_S(Z+1)}{2(Z-1)} \quad (35)$$

where

$$A_{00} = 1 - C_0, \quad A_{11} = 1 + C_0 \quad (36)$$

$$A_0 = 1 + a_0, \quad A_1 = 1 + b_0, \quad B_0 = a_0 - 1, \quad B_1 = b_0 - 1 \quad (37)$$

and

$$C_0 = \frac{2\tau_{RC}}{T_S}, \quad a_0 = \frac{2\tau_2}{T_S}, \quad b_0 = \frac{2\tau_1}{T_S} \quad (38)$$

Note that the Z -domain representation for $V(S)$ is exactly the same as Eq. (33), except that C_0 is replaced by

$$C_0 = \frac{2\tau_V}{T_S} \quad (39)$$

The digital closed-loop transfer function, $H(Z)$, for this case is given by

$$H(Z) = \frac{AK(B(Z)F(Z)V(Z)K(Z))}{[1 + AK(B(Z)F(Z)V(Z)K(Z))]} \quad (40)$$

Plots of the analog and digital closed-loop phase and magnitude responses are shown in Figs. 9(a) and 9(b). These figures show that for sampling frequencies below 100 kHz, distortions in phase and magnitude can occur for the digital approximation loop. In addition, the figures show that for sampling frequencies greater than or equal to 100 kHz the response of the digital loop approaches that of the analog counterpart. Hence, the minimum sampling frequency for this case is 100 kHz. Figures 10(a), (b), and (c) show the recursive implementation of the LPF $B(Z)$, integrator $K(Z)$, and loop filter $F(Z)$.

The implementation of the rolloff filter $V(Z)$ is similar to that of the LPF $B(Z)$.

2. Recursive Implementation of the Analog Transfer Function $G(S)$ and $K(S)$ Using Impulse-Invariant Transformation. To obtain the equivalent digital approximation for the integrator $K(S)$, one substitutes Eq. (29) into Eq. (26) to get

$$K(Z) = \frac{ZT_S}{(Z-1)} \quad (41)$$

The digital approximation for the analog transfer function $G(S)$ (see Eq. (27)) is obtained by finding the inverse Laplace transform of $G(S)$ and then substituting the result into Eq. (30). Evaluating Eq. (30), one has

$$G_D(Z) = T_S \left[\frac{\alpha_0}{1 - Z^{-1}e^{-aT_S}} + \frac{\alpha_1}{1 - Z^{-1}e^{-bT_S}} + \frac{\alpha_2}{1 - Z^{-1}e^{-cT_S}} \right] \quad (42)$$

where

$$\alpha_0 = \frac{\tau_1 - \tau_2}{(\tau_1 - \tau_{RC})(\tau_1 - \tau_V)} \quad (43)$$

$$\alpha_1 = \frac{\tau_{RC} - \tau_2}{(\tau_{RC} - \tau_1)(\tau_{RC} - \tau_V)} \quad (44)$$

$$\alpha_2 = \frac{\tau_V - \tau_2}{(\tau_2 - \tau_1)(\tau_V - \tau_{RC})} \quad (45)$$

and

$$a = \frac{1}{\tau_1}, \quad b = \frac{1}{\tau_{RC}}, \quad c = \frac{1}{\tau_V} \quad (46)$$

The digital closed-loop transfer function for this case is given by

$$H(Z) = \frac{AK(G_D(Z)K(Z))}{[1 + AK(G_D(Z)K(Z))]} \quad (47)$$

From Eq. (47), the plots of the phase and magnitude responses can be obtained for the digital approximation loop. Figures 11(a) and 11(b) illustrate the closed-loop phase and magnitude responses for both analog and digital loops. The figures show that the response of the digital loop approximated by using impulse-invariant transformation is the same as the analog loop when the sampling frequency is higher than or equal to 100 kHz. When the sampling frequency is less than 100 kHz, the digital loop can encounter serious distortion in both phase and amplitude. The recursive implementations $G_D(Z)$ and $K(Z)$ using impulse-invariant transformation are shown in Figs. 12(a) and 12(b).

3. Recursive Implementation of the Analog Transfer Function $G(S)$ and $K(S)$ Using Step-Invariant Transformation. Digital approximations $K(Z)$ and $G_D(Z)$ for $K(S)$ and $G(S)$ using step invariant transformation can be obtained by using Eqs. (31) and (32). The results are

$$K(Z) = \frac{T_s}{(Z - 1)} \quad (48)$$

$$\begin{aligned} G_D(Z) = & \beta_0 + \beta_1 \left[\frac{1 - Z^{-1}}{1 - Z^{-1}e^{-aT_s}} \right] \\ & + \beta_2 \left[\frac{1 - Z^{-1}}{1 - Z^{-1}e^{-bT_s}} \right] \\ & + \beta_3 \left[\frac{1 - Z^{-1}}{1 - Z^{-1}e^{-cT_s}} \right] \end{aligned} \quad (49)$$

where

$$\beta_0 = \frac{\alpha_0}{a} + \frac{\alpha_1}{b} + \frac{\alpha_2}{c} \quad (50)$$

$$\beta_1 = -\frac{\alpha_0}{a}, \beta_2 = -\frac{\alpha_1}{b}, \beta_3 = -\frac{\alpha_2}{c} \quad (51)$$

The parameters α_0 , α_1 , a , b , and c are defined in Eqs. (43)–(46), respectively. Again, Eq. (47) can be used to evaluate the closed-loop transfer function for this case. The plots of the closed-loop transfer functions for both analog and digital loops are shown in Figs. 13(a) and 13(b). The figures

show that the magnitude response approaches the analog response when the sampling frequency is higher than or equal to 100 kHz. However, the phase response suffers serious distortion when the sampling frequency is less than 1 MHz. Thus, in order to achieve the same response as the analog loop, the digital approximation loop using step-invariant transformation must be sampled at least at 1 MHz, i.e., this method requires a 10 times higher sampling frequency than the previous methods. The recursive implementations of $G_D(Z)$ and $K(Z)$ using step-invariant transformation are shown in Figs. 14(a) and 14(b).

V. Conclusions and Future Work

This article presented preliminary results on the design and implementation of the baseline digital baseband architecture for future deep space transponders, and also presented trade studies on: (1) the number of bits required by the ADC, (2) the sampling and IF for hardware simplification, and (3) the optimum sampling technique. A conceptual implementation of the proposed optimum sampling technique was presented and discussed. In addition, the phase and amplitude responses of digital approximations of the analog loop were briefly investigated. It was found that in order to achieve the same closed-loop responses as the analog counterpart, the step-invariant transformation method requires a higher sampling frequency than the other methods.

Furthermore, this article identified various architectures for possible implementation of the digital carrier tracking loop. The architecture that was found to provide the smallest phase jitter and fastest response is appropriate for the advanced transponder.

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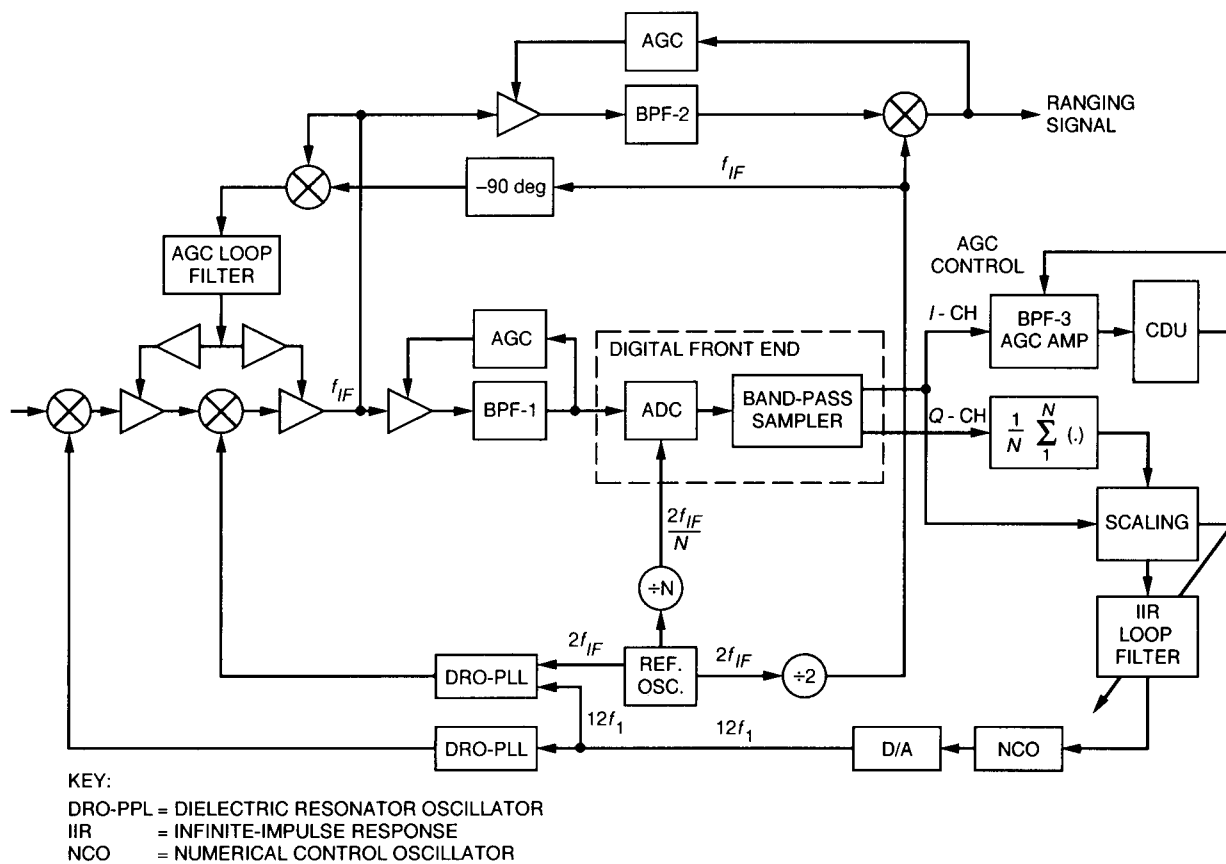


Fig. 1. Proposed baseline architecture for the advanced deep space transponder—a basic digital structure with analog turnaround ranging.

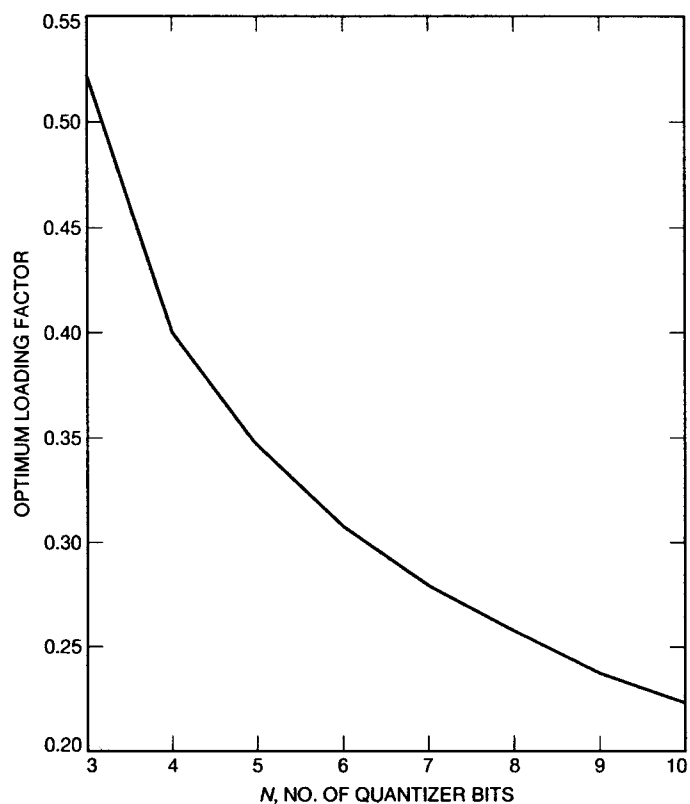


Fig. 2. Optimum loading factor as a function of N .

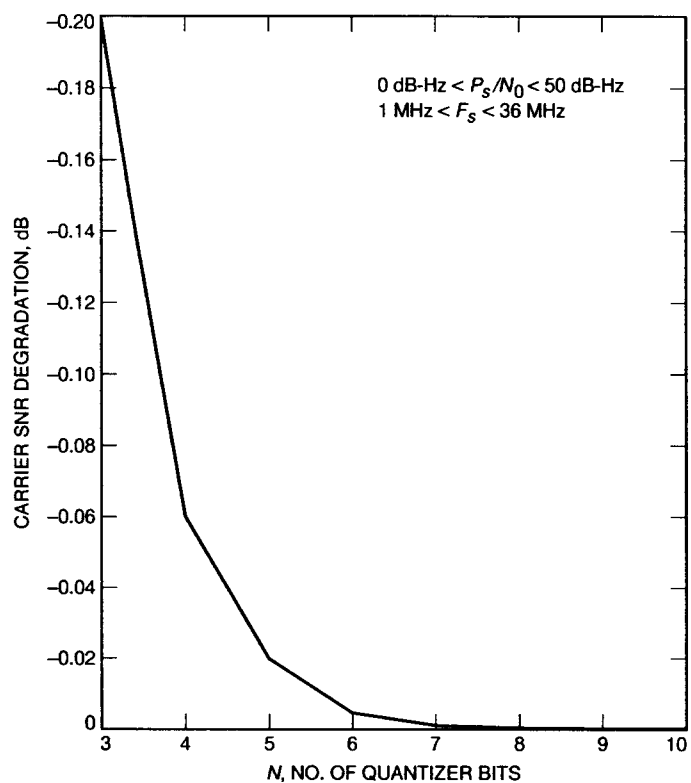


Fig. 3. Carrier SNR degradation as a function of N .

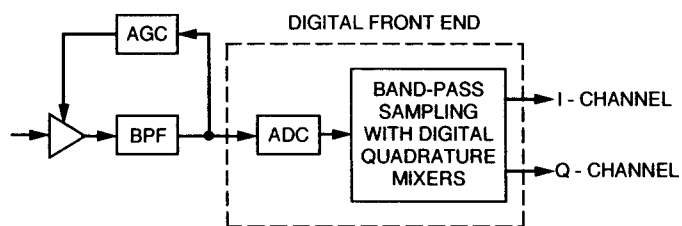


Fig. 4. A simplified block diagram of the proposed configuration for the digital front end of the transponder.

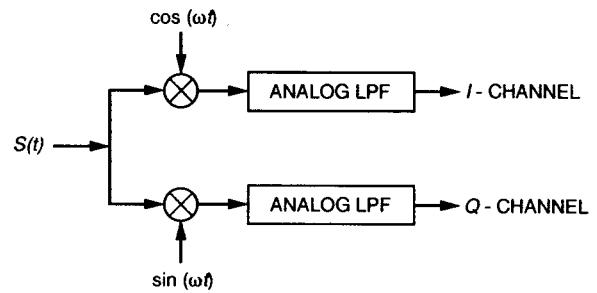
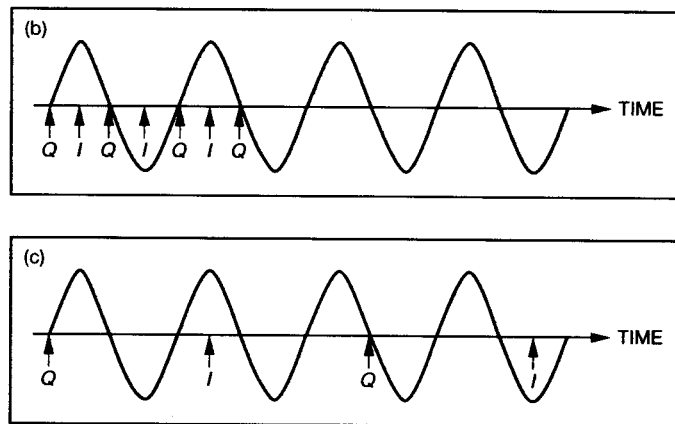


Fig. 6. I&Q extraction using the analog mixer approach.



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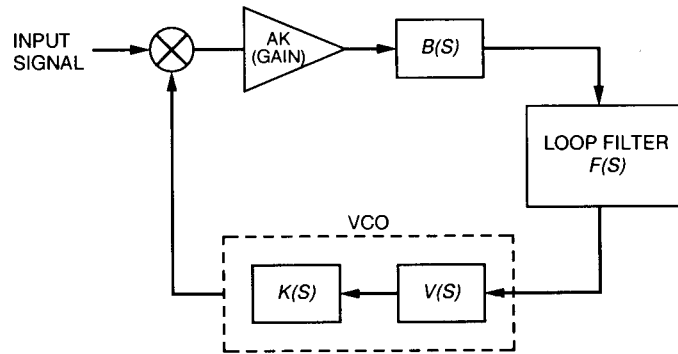


Fig. 8. Analog model of the Cassini carrier-tracking phase-locked loop—a short-loop version.

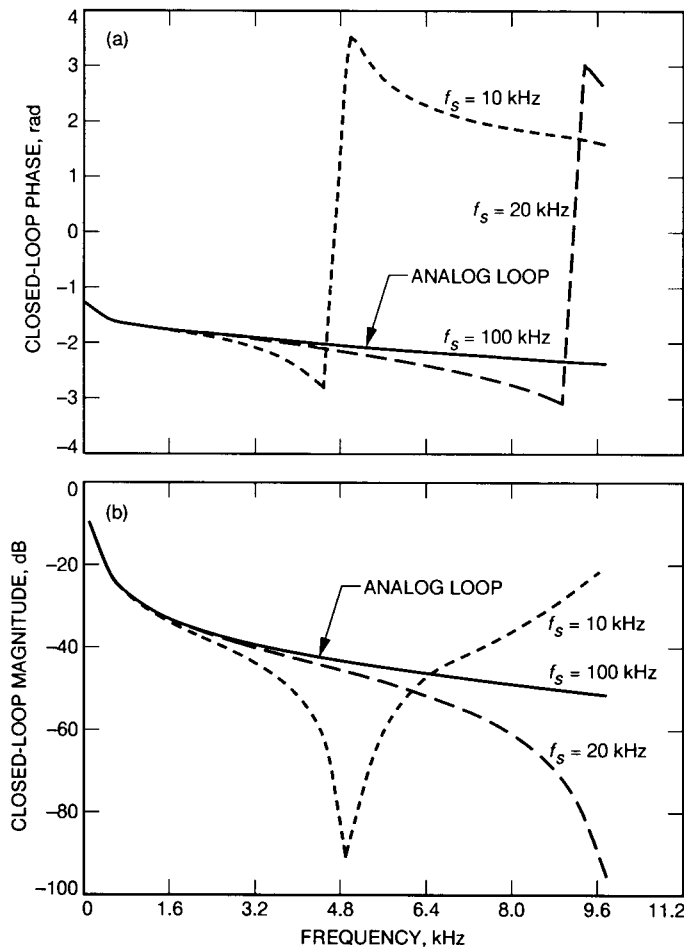


Fig. 9. Plots of two closed-loop responses for the digital loop using the bilinear transformation method: (a) phase response and (b) magnitude response.

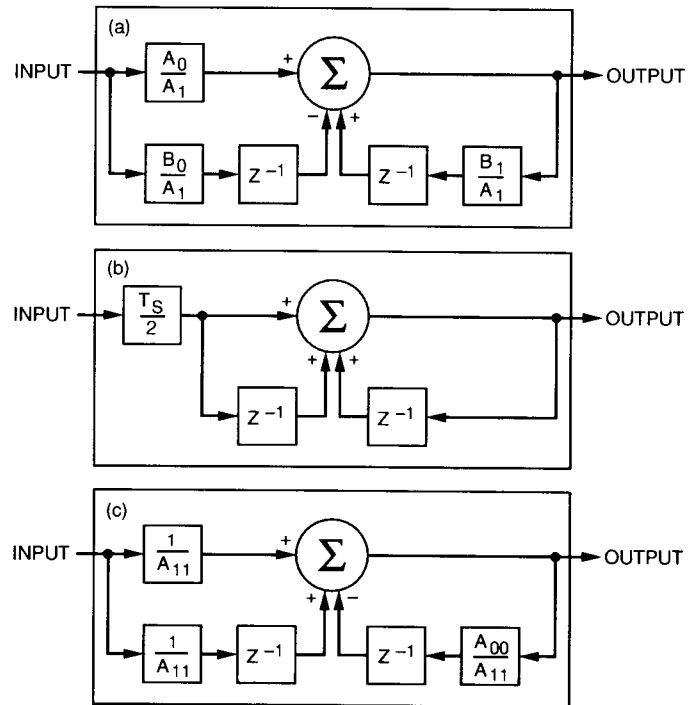


Fig. 10. Recursive implementation of the digital loop using the bilinear transformation method: (a) low-pass filter $B(Z)$, (b) integrator $K(Z)$, and (c) loop filter $F(Z)$.

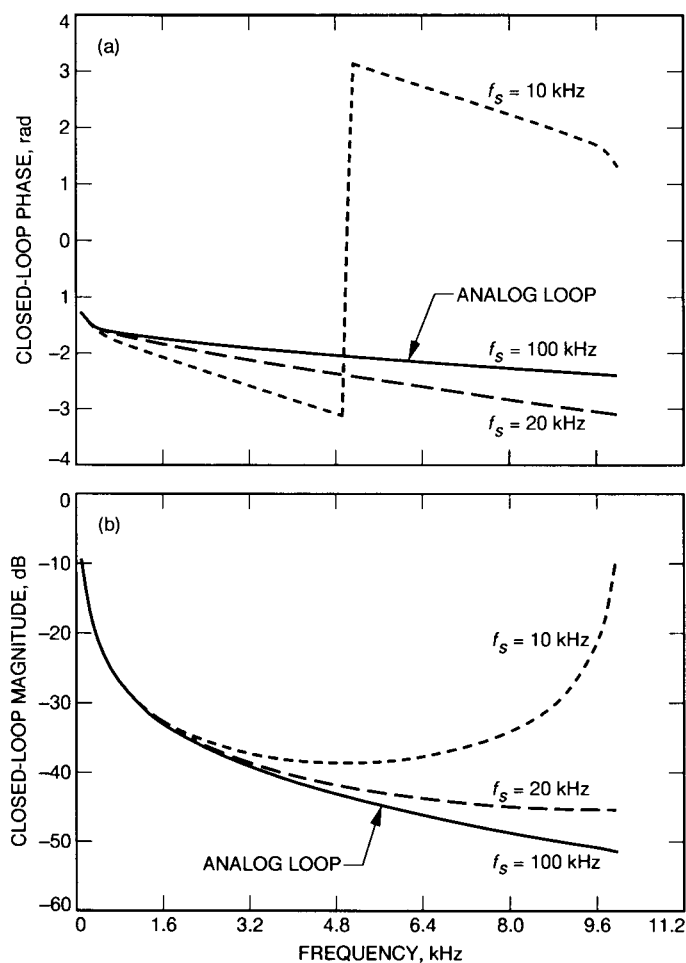


Fig. 11. Plots of two closed-loop responses for the digital loop using the impulse-invariant transformation method: (a) phase response and (b) magnitude response.

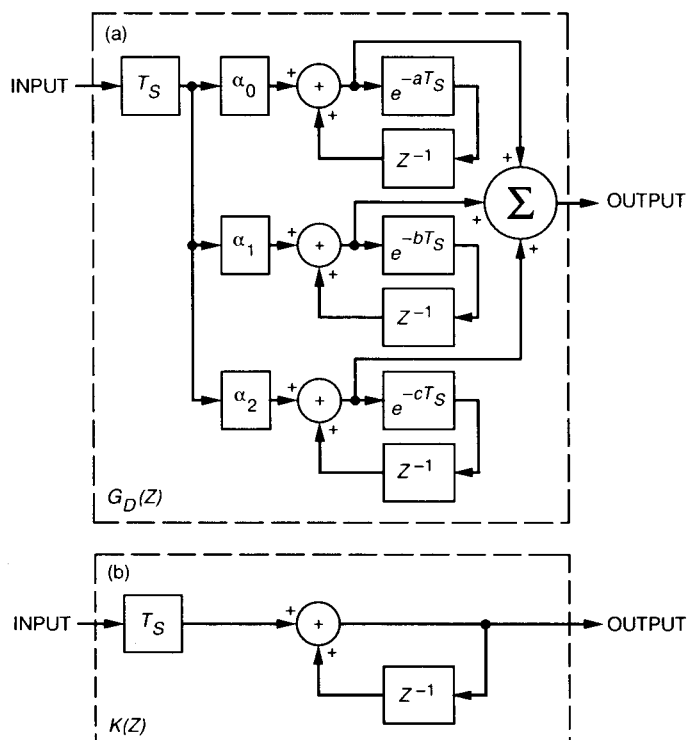


Fig. 12. Recursive implementation of the digital loop using the impulse-invariant transformation method: (a) open-loop transfer function $G_D(Z)$ and (b) integrator $K(Z)$.

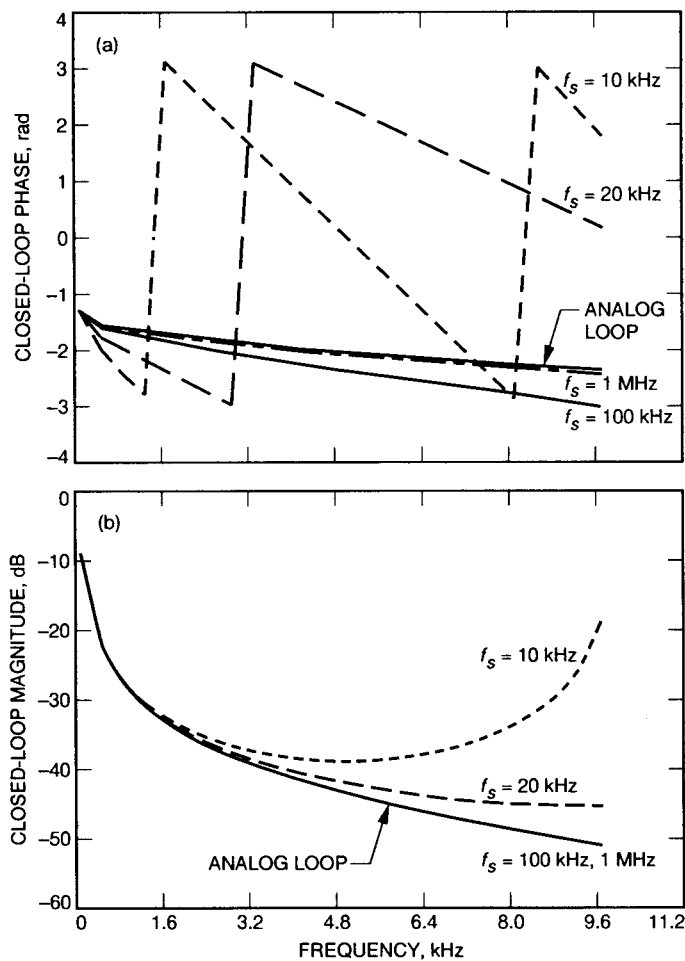


Fig. 13. Plots of two closed-loop responses for the digital loop using the step-invariant transformation method: (a) phase response and (b) magnitude response.

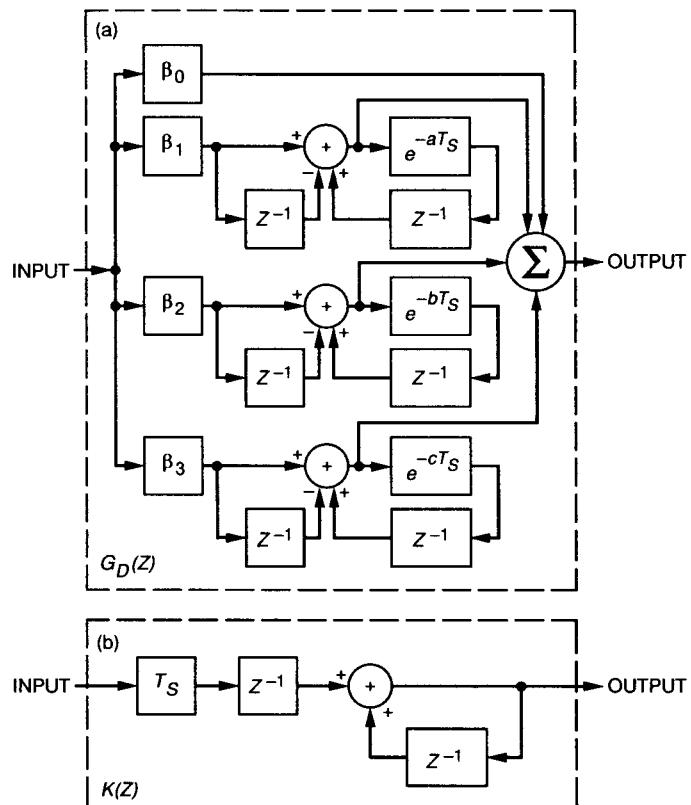


Fig. 14. Recursive implementation of the digital loop using the step-invariant transformation method: (a) open-loop transfer function $G_D(Z)$ and (b) integrator $K(Z)$.